Hall Ticket Number:

Code No. : 6136

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
M.E. (ECE: CBCS) I-Semester Main Examinations, Jan./Feb.-2017

(Embedded Systems & VLSI Design)

VLSI Technology

Time: 3 hours Max. Marks: 70

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Describe how capacitors can be realized in a CMOS process.
2. Describe the isolation techniques used in CMOS processes.
3. What are the major drawbacks of NMOS process?
4. Explain the structure of contacts to poly silicon and diffusion in submicron processes.
5. Explain why metallurgical grade silicon cannot be directly converted into electronic grade silicon.
6. Compare CVD based epitaxy and solid state epitaxy.
7. Define step coverage in deposition and discuss importance.
8. Compare wet and dry etching techniques.
9. What is basic difference between diffusion and ion implantation process?
10. Explain why clean rooms are needed for IC fabrication.

Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) List the major process steps in fabricating MOSFETs.
    b) Discuss why is the poly-silicon gate capacitance is much larger than metal to substrate capacitance per unit area.
12. a) Discuss the functions of epitaxial layer, poly-silicon layer and metal layer in CMOS ICs.
    b) Discuss why silicon is preferred as the base material for fabricating integrated circuits.
13. a) How does the pull rate in CZ process influence the crystal growth?
    b) Why silicon wafers are usually cleaned chemically prior to use? Discuss the typical cleaning process for silicon wafer.
14. a) Describe the stepper based technique of lithography discussing its advantages.
    b) Photo resist can be used as a mask for implantation and etching but cannot be used for oxidation and diffusion processes. Discuss why?
15. a) Describe the damage that happens during the implantation process discussing why the damage is created? Explain how it is removed?
    b) Discuss how junctions and transistor structures are formed in ICs using multiple diffusions.
16. a) Compare isolation techniques used in CMOS and bipolar ICs.
    b) Discuss the advantages of using poly-silicon as gate material in CMOS ICs.
17. Write short notes on any ***two*** of the following:
    a) Molecular beam epitaxy
    b) Electron beam lithography
    c) Packaging Techniques.

13. a) Derive stress- strain relationships for isotropic material. [4]

b) Derive the stress equilibrium equations from basic principles of 3D Elasticity [6]

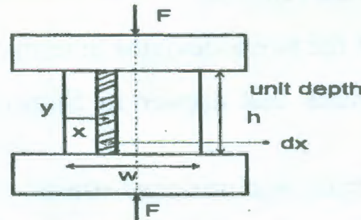
14. a) With respect to plasticity, Explain the following:- [5]

i) Yield criterion ii) Hardening Rule iii) Flow Rule

b) Describe Levy-Mises equations for rigid plastic material. [5]

15. a) What are the assumptions of slab method for forging analysis? [4]

b) A rectangular part having dimension: w x h x 1 forged in open die (see figure). [6]



Develop the expressions for variation of die pressure as given below:

$$p_x = 1.15 \cdot \sigma_{flow} \cdot \exp\left(\frac{2\mu x}{h}\right)$$

16. a) Show that the normal component of the stress vector on the octahedral plane is equal to one third the first invariant of the stress tensor. [5]

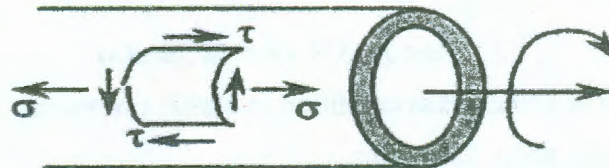
b) With the existence of continuous displacement functions **u** and **v**, show the following for 2D Elastic body:- [5]

$$\epsilon_x = \frac{\partial u}{\partial x}, \qquad \epsilon_y = \frac{\partial v}{\partial y}, \qquad \gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \qquad \frac{\partial^2 \epsilon_x}{\partial y^2} + \frac{\partial^2 \epsilon_y}{\partial x^2} = \frac{\partial^2 \gamma_{xy}}{\partial x\, \partial y}$$

17. Answer any *two* of the following:

a) Discuss the material matrix [D] for orthotropic material. [5]

b) The state of stress of thin walled tube is shown: - [5]



Sketch Von-mise's yield locus in(σ, τ) stress space.

c) Write the assumptions and limitations of Slip line field theory/method. [5]

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